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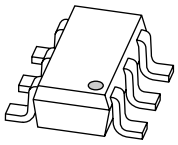


# PMN49EN

## N-channel TrenchMOS logic level FET

**Rev. 01 — 13 April 2007** **Product data sheet**

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Logic level threshold
- Fast switching

### 1.3 Applications

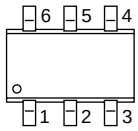
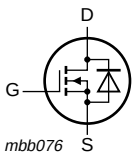
- Battery management
- High-speed switching

### 1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 4.6$ A
- $R_{DSon} \leq 47$ mΩ
- $Q_{GD} = 1.6$ nC (typ)

## 2. Pinning information

**Table 1. Pinning**

| Pin | Description | Simplified outline | Symbol |
|---|---|---|---|
| 1, 2, 5, 6 | drain (D) |   SOT457 (TSOP6) |   |
| 3 | gate (G) | | |
| 4 | source (S) | | |

## 3. Ordering information

**Table 2. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PMN49EN | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

## 4. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 150 °C | - | 30 | V |
| $V_{DGR}$ | drain-gate voltage (DC) | 25 °C ≤ $T_j$ ≤ 150 °C; $R_{GS}$ = 20 kΩ | - | 30 | V |
| $V_{GS}$ | gate-source voltage | | - | ±20 | V |
| $I_D$ | drain current | $T_{sp}$ = 25 °C; $V_{GS}$ = 10 V; see Figure 2 and 3 | - | 4.6 | A |
| | | $T_{sp}$ = 100 °C; $V_{GS}$ = 10 V; see Figure 2 | - | 2.9 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs; see Figure 3 | - | 18.4 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C; see Figure 1 | - | 1.75 | W |
| $T_{stg}$ | storage temperature | | –55 | +150 | °C |
| $T_j$ | junction temperature | | –55 | +150 | °C |
| **Source-drain diode** | | | | | |
| $I_S$ | source current | $T_{sp}$ = 25 °C | - | 1.4 | A |
| $I_{SM}$ | peak source current | $T_{sp}$ = 25 °C; pulsed; $t_p$ ≤ 10 µs | - | 5.6 | A |



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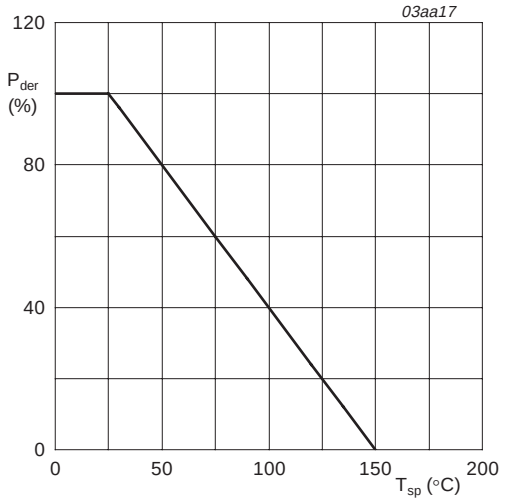
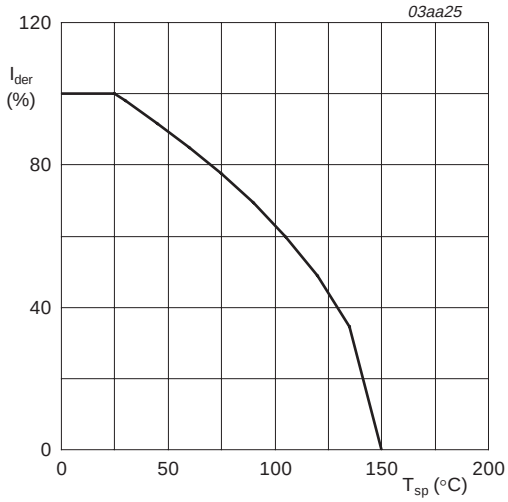


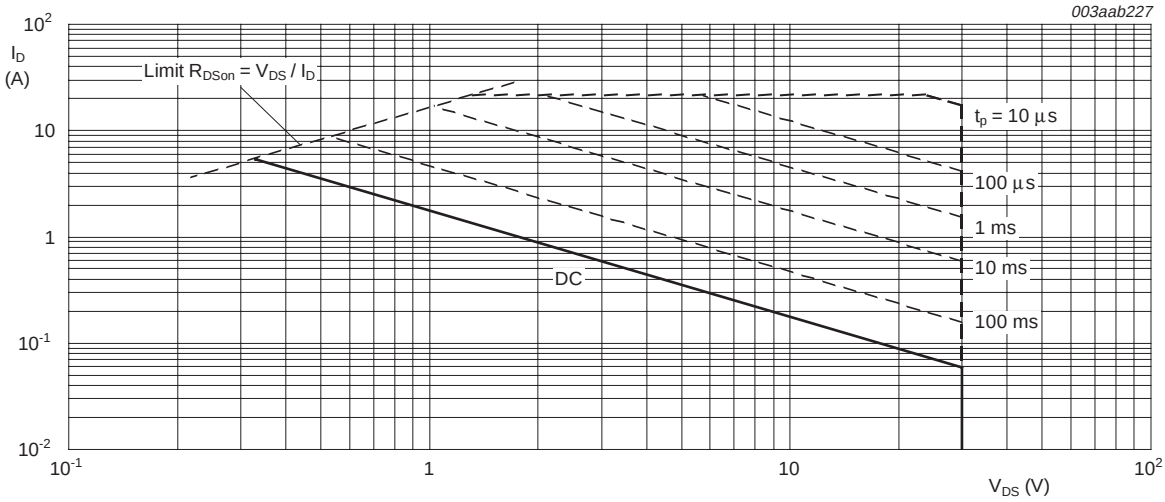

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig 1. Normalized total power dissipation as a function of solder point temperature**




$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

**Fig 2. Normalized continuous drain current as a function of solder point temperature**




$T_{sp}$ = 25 °C; $I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



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## 5. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see Figure 4 | - | - | 70 | K/W |

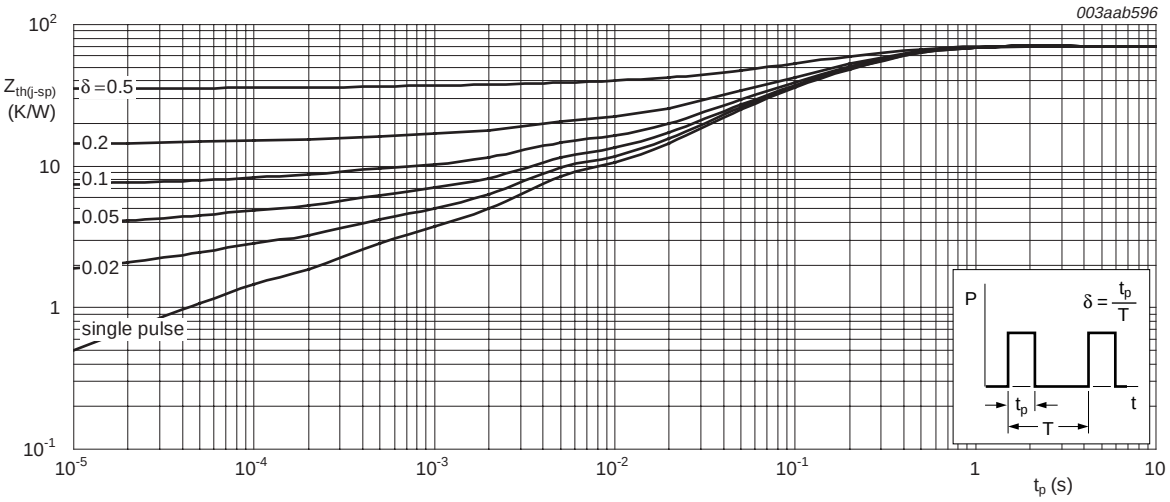


**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration**


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# 6. Characteristics

**Table 5. Characteristics**

*$T_j$ = 25 °C unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | 30 | - | - | V |
| | | $T_j$ = –55 °C | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; see Figure 9 and 10 | | | | |
| | | $T_j$ = 25 °C | 1 | 1.5 | 2 | V |
| | | $T_j$ = 150 °C | 0.6 | - | - | V |
| | | $T_j$ = –55 °C | - | - | 2.2 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 30 V; $V_{GS}$ = 0 V | | | | |
| | | $T_j$ = 25 °C | - | - | 1 | µA |
| | | $T_j$ = 150 °C | - | - | 100 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = ±20 V; $V_{DS}$ = 0 V | - | 10 | 100 | nA |
| $R_G$ | gate resistance | f = 1 MHz; $V_{GSS(AC)}$ = 150 mV | - | 1.9 | - | Ω |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 2 A; see Figure 6 and 8 | | | | |
| | | $T_j$ = 25 °C | - | 40 | 47 | mΩ |
| | | $T_j$ = 150 °C | - | 68 | 80 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 1.5 A; see Figure 6 and 8 | - | 49 | 60 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 3 A; $V_{DS}$ = 15 V; $V_{GS}$ = 4.5 V; see Figure 11 and 12 | - | 8.8 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 1.1 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 1.6 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | | - | 2.83 | - | V |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 30 V; f = 1 MHz; see Figure 14 | - | 350 | - | pF |
| $C_{oss}$ | output capacitance | | - | 100 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 64.1 | - | pF |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 0 V; f = 1 MHz | - | 570 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 15 V; $R_L$ = 15 Ω; $V_{GS}$ = 10 V; $R_G$ = 6 Ω | - | 4.1 | - | ns |
| $t_r$ | rise time | | - | 4.3 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 12.9 | - | ns |
| $t_f$ | fall time | | - | 4.9 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 1.5 A; $V_{GS}$ = 0 V; see Figure 13 | - | 0.79 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 2 A; $dI_S/dt$ = –100 A/µs; $V_{GS}$ = 0 V | - | 19.25 | - | ns |
| $Q_r$ | recovered charge | | - | 0.73 | - | nC |



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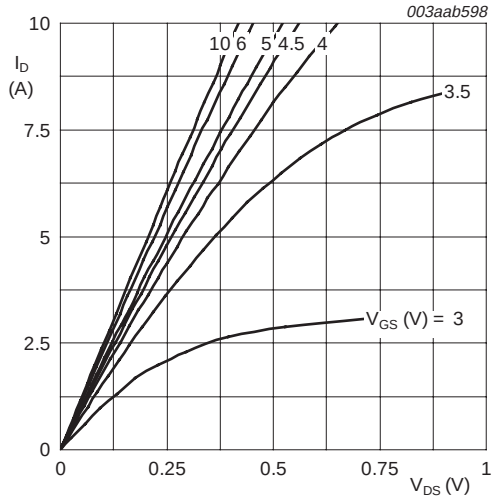
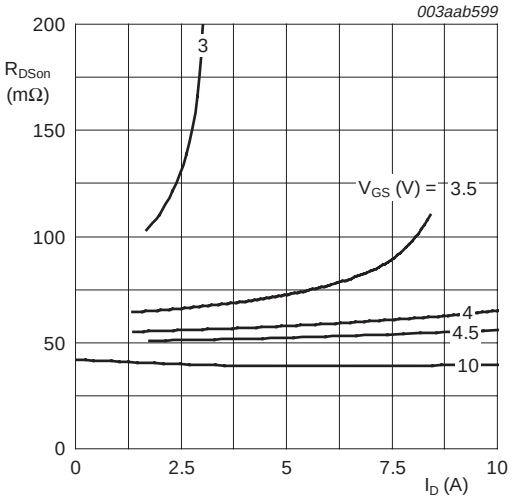



$T_j$ = 25 °C

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**




$T_j$ = 25 °C

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**

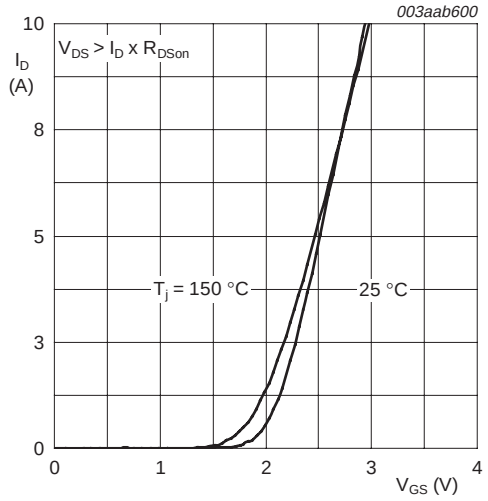
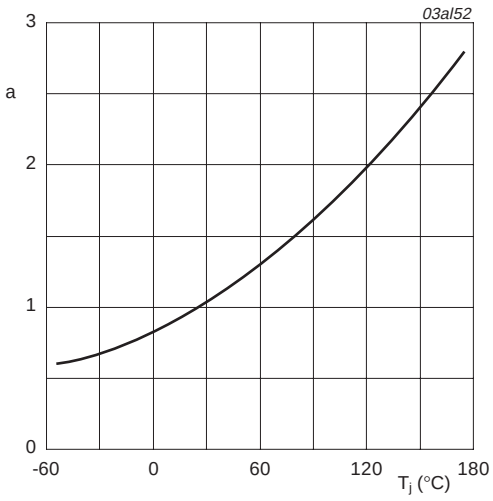



**Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values**




$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature**



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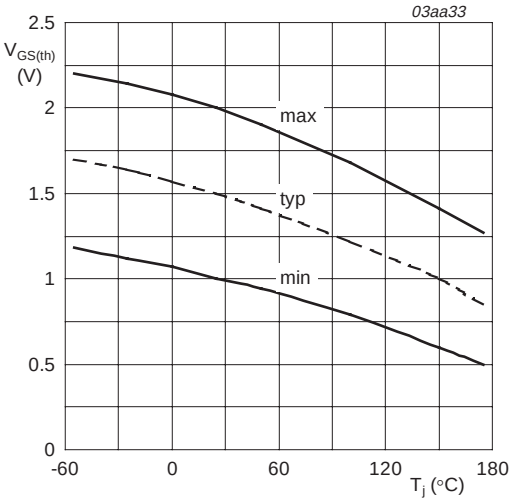
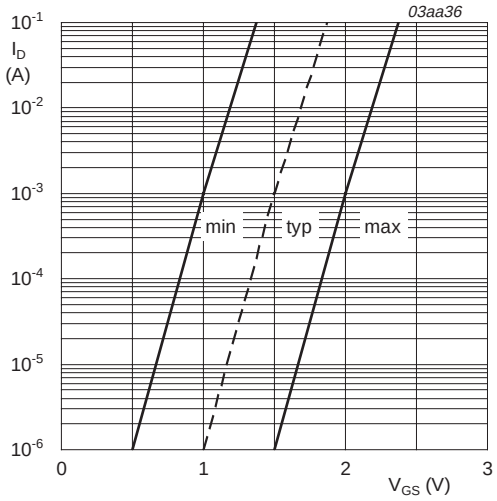



$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature**




$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig 10. Sub-threshold drain current as a function of gate-source voltage**

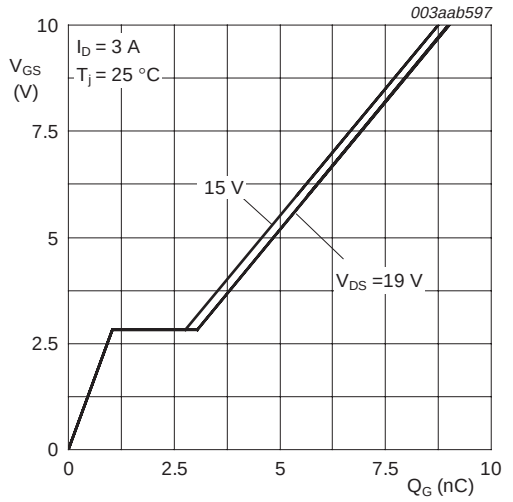



**Fig 11. Gate-source voltage as a function of gate charge; typical values**

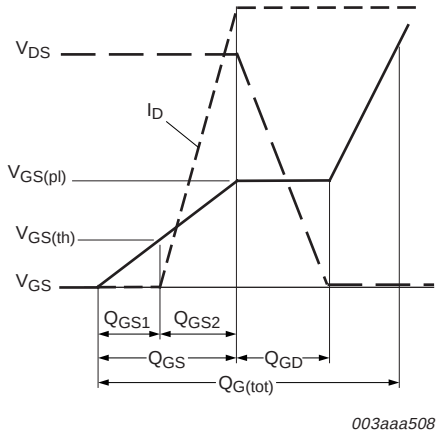



**Fig 12. Gate charge waveform definitions**



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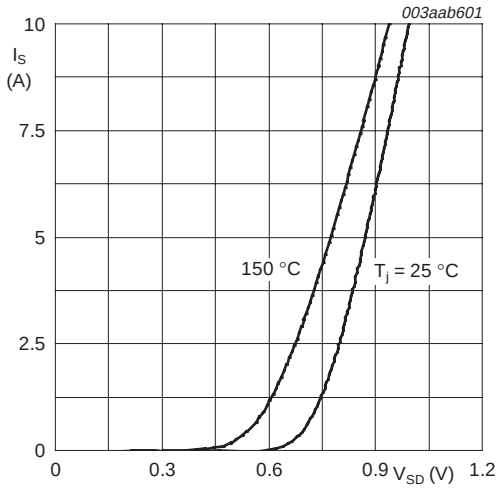
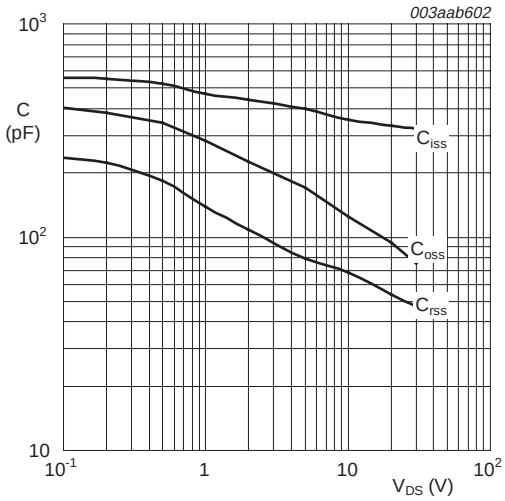



$T_j$ = 25 °C and 150 °C; $V_{GS}$ = 0 V

**Fig 13. Source current as a function of source-drain voltage; typical values**




$V_{GS}$ = 0 V; f = 1 MHz

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



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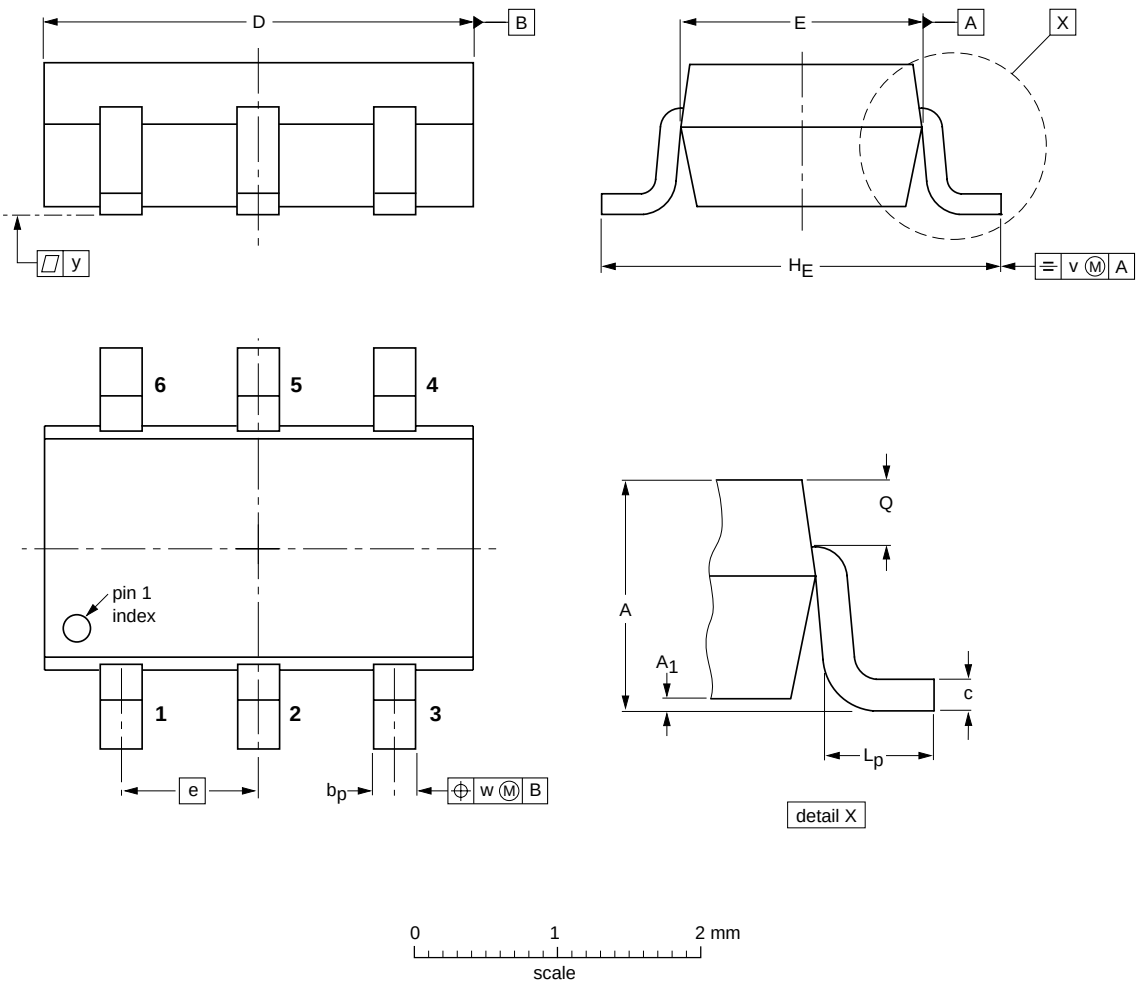
## 7. Package outline

**Plastic surface-mounted package (TSOP6); 6 leads** **SOT457**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT457 | | | SC-74 | | | ~~05-11-07~~<br>06-03-16 |

**Fig 15. Package outline SOT457 (TSOP6)**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## 8. Revision history

**Table 6. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PMN49EN_1 | 20070413 | Product data sheet | - | - |


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